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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,463	12/04/2003	Maximing Aguilar JR.	END920030111US1	1258

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EXAMINER	
TRUONG, CAMQUY	
ART UNIT	PAPER NUMBER
2195	

NOTIFICATION DATE	DELIVERY MODE
04/29/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/729,463	AGUILAR ET AL.	
	Examiner	Art Unit	
	CAMQUY TRUONG	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 Februalry 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-10,16,17 and 19-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-10, 16-17,and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6, 8-10, 16-17, 19-23 are presented for examination. Claims 7, 11-15 and 18 have been cancelled.

Continued Examination under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after the final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/9/09 has been entered.

Response to the argument

3. Applicant's arguments filed with RCE with respect to claims 1-6, 8-10, 16-17, 19-23 have been considered but are moot in view of the new ground(s) rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 1-6, 8-10, 16-17, 19-23 are rejected under 35 U.S.C 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. The claim language in the following claims is not clearly understood

i. As to claim 1,(line 17), claim 8 (line 19), claim 16 (line 21), it is not clearly indicated whether " the one or more executed tasks" refers to " the one or more tasks"; claim 1 (lines 16-17), claim 8 (lines 19-20) and claim 16 (lines 22-23), it is not clearly indicated whether " one or more temporal related tasks" refers to " one or more atomic sub-task" and how " one or more temporal related tasks" relates to " one or more atomic sub-task". If it is the same Applicant should use the same language.

ii. As to claim 16, line 22, it is not clearly indicated whether "a central task queue" refers to "a central task queue" in line 10.

iii. Claims 2-6, 9-10, 17, 19-23 do not cure the deficiency of claims 1, 8 and 16 above, therefor; they are rejected for the same reason above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-6, 8-10, 16-17, 19-22, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (U.S. Patent Application Publication. 2001/0051971 A1) in view of Magee et al. (U.S. Patent 5,729,710) and further in view of Matsui et al. (U.S. 2002/0010732 A1).**

6. As to claims 1 and 8, Kato teaches the invention substantially as claimed including: a method of task management comprising the steps of:

b. atomizing the one or more tasks into one or more atomic sub-tasks (breaking down a processing task into a plurality of self-contained task objects, paragraph 16, lines 1-2); and

c. assigning protection attributes indicating a portion of one of the memory ranges of the shared memory for each respective atomic sub-task of the one or more atomic sub-tasks (the master task grouping maintains an internal space address assigned to each respective task object, paragraph 21, lines 9-10; paragraph 56) such that each respective sub-task is executed by one of the plurality of processors which inherits access rights to the shared memory indicated by the protection attributes corresponding the respective atomic sub-task (accessing to the correct memory space address can be performed in a safe manner, paragraph 64/ the task object is assign to the unoccupied processor for executing, paragraph 19; paragraph. It is inherited that in order for the processor to execute the task object, the processor has to access to space address assigned to respective task object).

7. Kato does not explicitly teaches executing multiple instances of a kernel; generating one or more tasks to be executed from a plurality of the instance of the kernel, and wherein each of the protection attributes corresponding to a common instance of the multiple instance of the kernel is assigned such that the inherited access rights of the one or more processors which relate to respective sub-tasks derived from a respectively different common instance corresponds to a respectively different one o the memory ranges of the shared memory.

8. However, Magee teaches executing multiple instances of a kernel (col. 10, lines 54-67; col. 11, line 51 – col. 12, line 4; col. 13, lines 6-21); generating one or more tasks to be executed from a plurality of the instance of the kernel (col. 14, lines 41-44; col. 22, lines 9-2), and wherein each of the protection attributes corresponding to a common instance of the multiple instance of the kernel is assigned (task A may have a template region mapped at address hex4000, but task B may have the same template region mapped at template region mapped at address hex800F000, col. 47, lines 7-12; col. 12, lines 35-39; col. 33, line 1 – col. 34, line 29) such that the inherited access rights of the one or more processors which relate to respective sub-tasks derived from a respectively different common instance corresponds to a respectively different one o the memory ranges of the shared memory (col. 43, lines 50-59; col. 44, lines 17-31; col. 45, lines 4-22).

9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Kato by incorporating the teaching of executing multiple instances of a kernel; generating one or more tasks to be executed from a plurality of the instance of the kernel, and wherein each of the protection attributes corresponding to a common instance of the multiple instance of the kernel is assigned such that the inherited access rights of the one or more processors which relate to respective sub-tasks derived from a respectively different common instance corresponds to a respectively different one o the memory ranges of the shared memory as taught by Magee because this would provide enhanced security for tasks.

10. Kato and Magee do not explicitly teach generating one or more temporal related task from one or more executed tasks, and prioritizing and connecting the one or more temporal related tasks by their temporal relationship and insert the temporal related tasks into a central task queue to be executed according to their temporal relationship by one or more of the plurality of processor.

11. However, Matsui teaches generating one or more temporal related task from one or more executed tasks (when the parallel program manager 6 generates and allocates parallel processes of a parallel program, additionally, it generates dummy processes, paragraphs 136 and 142) and prioritizing and connecting the one or more temporal related tasks by their temporal relationship (the processes in the process queues 3 are sequenced by identifiers x and w assigned to them, the parallel processes of one of the

parallel programs are in the corresponding position of order in the process queues of the processors P1 and P2, paragraph 150) and insert the temporal related tasks into a central task queue to be executed according to their temporal relationship by one or more of the plurality of processor (the dummy process identifier w, placed in the process queues 3 of the processors, paragraph 150).

12. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Kato and Magee by incorporating the teaching of generating one or more temporal related task from one or more executed tasks, and prioritizing and connecting the one or more temporal related tasks by their temporal relationship and insert the temporal related tasks into a central task queue to be executed according to their temporal relationship by one or more of the plurality of processor as taught by Matsui because this would allow to schedule the run of parallel processes without requiring explicit processor-to-processor communication, thus reducing the overhead for coordination of the processors due to scheduling by coordinating the process-run steps of the processors.

13. As to claims 2-3, Matsui teaches scheduling the one or more atomic sub-tasks into a central task queue (paragraph 150).

14. As to claims 4-6, Kato teaches obtaining from a first idle processor of a plurality of processors a first atomic sub-task from the central task queue (all task objects in the

active states from any of the spaces are placed on the queue, and each is assigned in turn to a next available unoccupied processor, paragraph 21), the first idle processor thereby inheriting the access rights to one or more computing resources of the first atomic sub-task in executing the first atomic sub-task (when all of its defined data-waiting slots have been filled, it is assigned to a next available processor, paragraph 19. It is inherited that in order for the processor to execute the task object, the processor has to access to space address assigned to respective task object).

15. As to claim 9, Kato teaches a central task queue for storing the one or more atomic sub-tasks waiting to be executed (all task objects in the active state from any of the task spaces are placed on the queue, and each is assigned in turn to a next available processor, paragraph 21, lines 4-7).

31. As to claim 10, Matsui teaches a task scheduler for arranging the one or more atomic sub-tasks in the central task queue (The processes placed in the process queue 3 are arranged, according to the sequence of the identifiers assigned to the processes, Paragraph 73).

16. As to claim 16, Kato teaches method of task management comprising the steps of:

a. receiving one or more tasks to be executed (allocate the many tasks of the overall processing work among the processors so that none are overloaded or

excessively idle, paragraph 5, lines 14-17/ performing processing task in parallel on a plurality of processors comprises: breaking down a processing task into a ..., paragraphs 15 – 16. it is inherit that in order to perform processing task in parallel on a plurality of processors, the processing task has to be received);

b. atomizing the one or more tasks into one or more atomic sub-tasks (breaking down a processing task into a plurality of self-contained task objects, paragraph 16, lines 1-2);

c. assigning protection attributes indicating a memory range of a shared memory for each respective atomic sub-task of the one or more atomic sub-tasks (the master task grouping maintains an internal space address assigned to each respective task object, paragraph 21, lines 9-10; paragraph 56) such that each respective sub-task is executed by one of the plurality of processors which inherits access rights to the shared memory indicated by the protection attributes corresponding the respective atomic sub-task (accessing to the correct memory space address can be performed in a safe manner, paragraph 64/ the task object is assign to the unoccupied processor for executing, paragraph 19; paragraph. It is inherited that in order for the processor to execute the task object, the processor has to access to space address assigned to respective task object);

e. obtaining via a first idle processor of a plurality of processors a first atomic sub-task from the central task queue for execution of the first atomic sub-task (all task objects in the active states from any of the spaces are placed on the queue, and each is assigned in turn to a next available unoccupied processor, paragraph 21); and

f. obtaining via a further idle processor of the plurality of processors a further atomic sub-task from the central task queue (all task objects in the active states from any of the spaces are placed on the queue, and each is assigned in turn to a next available unoccupied processor, paragraph 21).

17. Kato does not explicitly teaches executing multiple instances of a kernel; generating one or more tasks to be executed from a plurality of the instance of the kernel, and wherein each of the protection attributes corresponding to a common instance of the multiple instance of the kernel is assigned such that the inherited access rights of the one or more processors which relate to respective sub-tasks derived from a respectively different common instance corresponds to a respectively different one o the memory ranges of the shared memory.

18. However, Magee teaches each of the protection attributes corresponding to a common instance of the multiple instance of the kernel is assigned (A task A may have a template region mapped at address hex4000, but task B may have the same template region mapped at template region mapped at address hex800F000, col. 47, lines 7-12; col. 12, lines 35-39; col. 33, line 1 – col. 34, line 29) such that the inherited access rights of the one or more processors which relate to respective sub-tasks derived from a respectively different common instance corresponds to a respectively different one o the memory ranges of the shared memory (col. 43, lines 50-59; col. 44, lines 17-31; col. 45, lines 4-22).

19. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Kato by incorporating the teaching of each of the protection attributes corresponding to a common instance of the multiple instance of the kernel is assigned such that the inherited access rights of the one or more processors which relate to respective sub-tasks derived from a respectively different common instance corresponds to a respectively different one o the memory ranges of the shared memory as taught by Magee because this would enhance security for tasks.

20. Kato and Magee do not explicitly teach scheduling the one or more atomic sub-tasks into a central task queue according to one or both of temporal and priority considerations and generating one or more temporal related task from one or more executed tasks, and prioritizing and connecting the one or more temporal related tasks by their temporal relationship and insert the temporal related tasks into a central task queue to be executed according to their temporal relationship by one or more of the plurality of processor.

21. However, Matsui teaches scheduling the one or more atomic sub-tasks into a central task queue according to one or both of temporal and priority considerations. (the processes in the process queues 3 are sequenced by identifiers x and w assigned to them, the parallel processes of one of the parallel programs are in the corresponding

position of order in the process queues of the processors P1 and P2, paragraph 150) and generating one or more temporal related task from one or more executed tasks (when the parallel program manager 6 generates and allocates parallel processes of a parallel program, additionally, it generates dummy processes, paragraphs 136 and 142) and prioritizing and connecting the one or more temporal related tasks by their temporal relationship (the processes in the process queues 3 are sequenced by identifiers x and w assigned to them, the parallel processes of one of the parallel programs are in the corresponding position of order in the process queues of the processors P1 and P2, paragraph 150) and insert the temporal related tasks into a central task queue to be executed according to their temporal relationship by one or more of the plurality of processor (the dummy process identifier w, placed in the process queues 3 of the processors, paragraph 150).

22. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Kato and Magee by incorporating the teaching of scheduling the one or more atomic sub-tasks into a central task queue according to one or both of temporal and priority considerations and generating one or more temporal related task from one or more executed tasks, and prioritizing and connecting the one or more temporal related tasks by their temporal relationship and insert the temporal related tasks into a central task queue to be executed according to their temporal relationship by one or more of the plurality of processor as taught by Matsui because this would allow to schedule the run of parallel processes without

requiring explicit processor-to-processor communication, thus reducing the overhead for coordination of the processors due to scheduling by coordinating the process-run steps of the processors.

23. As to claims 17 and 19, Matsui teaches scheduling the one or more atomic sub-tasks into a central task queue is done according to temporal considerations (paragraph 150).

24. As to claim 20, Matsui teaches scheduling the one or more atomic sub-tasks into a central task queue is done according to priority considerations (a procedure for generating and storing a queue of processes specified to be executed on each processor, claim 5).

25. As to claim 21, Kato teaches:

Designating a master kernel (col. 10, lines 54-56);

Submitting, by the multiple instances of the kernel, the one or more atomic sub-tasks to the master kernel (allocate the many tasks of the overall processing work among the processors so that none are overloaded or excessively idle, paragraph 5, lines 14-17/ performing processing task in parallel on a plurality of processors comprises: breaking down a processing task into a …, paragraphs 15 – 16. it is inherit

that in order to perform processing task in parallel on a plurality of processors, the processing task has to be received); and

placing the one or more sub-tasks into a central task-queue after the consolidating step (paragraph 21)

Magee teaches:

scheduling, by the master kernel, all of the multiple other instances of the kernel (col. 20, lines 29-33);

consolidating priority and temporal execution parameters of each sub-task (col. 20, lines 29-43).

26. As to claim 22, Kato teaches:

determining whether any of the plurality of processors are idle (paragraph 19);

responsive to the of the processors being idle, receiving, by the processor determined to be idle, a first atomic sub-task using, the shared memory designated by the corresponding protection attribute (allocate the many tasks of the overall processing work among the processors so that none are overloaded or excessively idle, paragraph 5, lines 14-17/ performing processing task in parallel on a plurality of processors comprises: breaking down a processing task into a ..., paragraphs 15 – 16. it is inherit that in order to perform processing task in parallel on a plurality of processors, the processing task has to be received);

repeatedly and simultaneously determining whether another processor is idle and executing a subsequent atomic sub-task until all tasks are completed (paragraph 48).

27. **Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (U.S. Patent Application Publication. 2001/0051971 A1) in view of Magee et al. (U.S. Patent 5,729,710, and further in view of Matsui et al. (U.S. 2002/0010732 A1) as applied to claim 22 above, and further in view of Martin (U.S. Patent 4,466,064).**

28. As to claim 23, Kato, Mage and Matsui do not explicitly teach:

providing the summing junction as part of the kernel; and routing the combined execution results of the completed task to an input/output port for delivery to a calling process. However, Martin teaches:

providing a summing junction as part of the kernel; (col. 8, lines 21-24); and

routing the combined execution results of the completed task to an input/output port for delivery to a calling process (col. 8, lines 24-27).

29. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Kato, Magee and Matsui by incorporating the teaching of providing a summing junction as part of the kernel; combining the execution results of each of the atomic sub-tasks for a completed task using the summing junction; and routing the combined execution results of the completed task to an input/output port for delivery to a calling process as taught by Martin because this would improve system's performance while executing plurality of tasks.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAMQUY TRUONG whose telephone number is (571)272-3773. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai An can be reached on (703)305-9678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/VAN H NGUYEN/
Primary Examiner, Art Unit 2194

Camquy Truong

April 23, 2009